Dr. Asmy Kumari
Dept. of Physics
H. D. Jain college, Ara

PG III semester

Paper - CC12, unit -

Topic - BCD Decade Counter

Other Uses of this Circuit:-

(i) To decode a count of 13: Refer to the table 1(c). At count 13, $Q_A = 1$, $Q_B = 0$, $Q_C = 1$, $Q_D = 1$. Therefore to get a count of 13, we use a four input AND gate with $Q_A$, $Q_B$, $Q_C$ and $Q_D$ as input. All inputs are a 1, i.e. $Q_A = 1$, $Q_B = 1$, $Q_C = 1$, $Q_D = 1$ so that $\overline{Q}_B = 0$.

Thus we apply 1101 at the input of AND gate and get a count of 13. We note that most significant bit (MSB) is D while least significant bit (LBS) is A (fig 19).

(ii) As frequency divider:- from fig 1(b), it is clear that the frequency of output

DATE / /

from A is one half that of CP and the frequency of output from B is one-quarter that of CP. It leads to the way of designing 'divide by' counters, e.g. 'divide by 60' etc.

## BCD Decade counter

A binary coded decimal (BCD) counter is shown in fig (2). The counter will reset itself to zero after a count of 10. forced feedback is used to return the counter to a reset state after nine natural binary counts. On count 10, all the outputs are low, i.e. outputs of all flip flops are 0. Truth table for this counter is thus same as for a scale of 16 counter upto and including count 9.

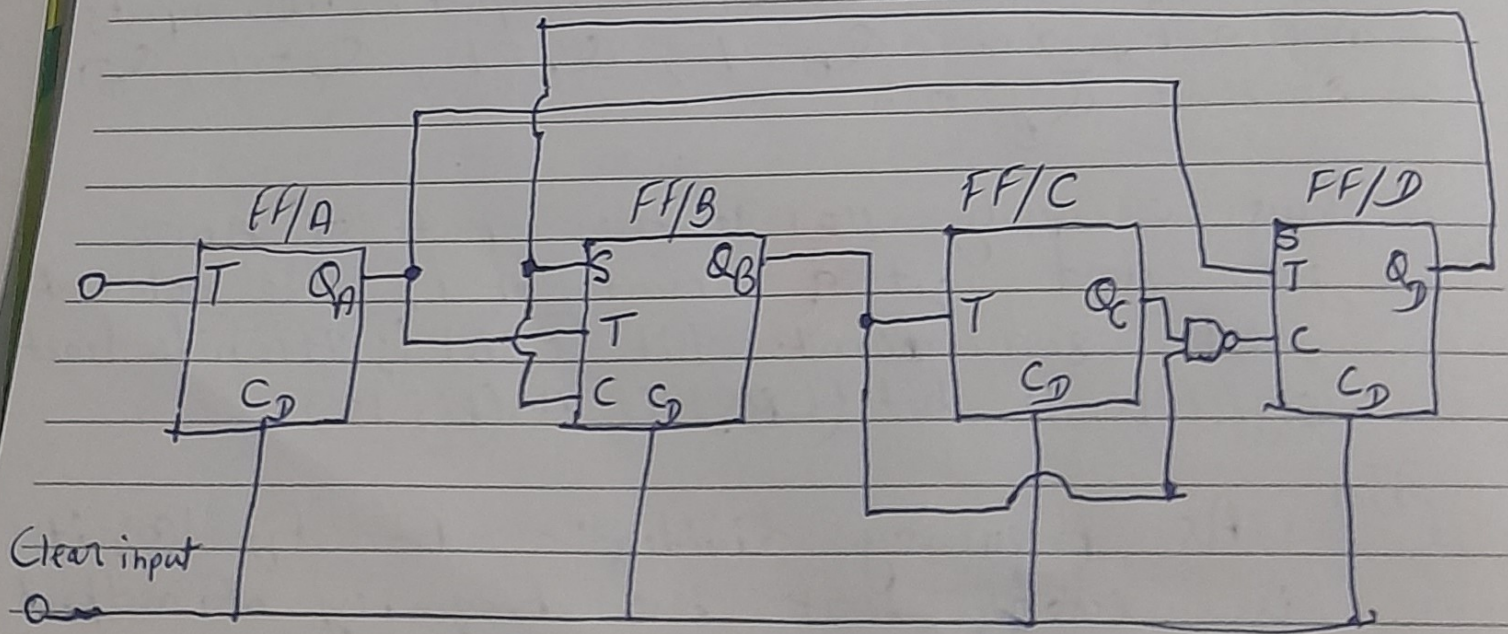


fig 2. A BCD decade counter.

DATE ___/___/___

The operation can be briefed with the help of truth table fig(1b) as follows:

(i) At the falling edge of every CP, flip flop A changes its state i.e. from a 1 to a 0, and vice versa.

(ii) Flip flop C changes its state ~~everything~~ everytime B changes from a 1 to a 0, i.e. at the falling edge of $Q_B$ fig 1(b). Thus triggering of flip flop C depends upon the output of B.

(iii) Flip flop B changes its state when $Q_A$ goes from a 1 to a 0 (i.e. at the falling edge of $Q_A$. fig 1(b)), except on tenth pulse. From fig 1(b), we note that though at falling edge of tenth pulse $Q_A$ goes from a 1 to a 0 but $Q_B$ will not rise from a 0 to a 1. The reason is that because now $Q_D$ has also become a 1 and as it is fedback to the input of B, the input of B remains high (a 1) and thus its output $Q_B$ cannot change its state. i.e. it continues to be a low (a 0).

In otherwords B, its inhibited from

changing back to a 1 at this time.

Thus at the arrival of ~~tenth~~ tenth pulse, $Q_A$ goes from a 1 to a 0, $Q_B$ is forced to 0, and $Q_C = 0$ (already low). Since $Q_B = 0$, $Q_C = 0$ there will a 1 at the clear input, $C_1$, of the flip flop D so that $Q_D$ will also be a 0. Thus Q output of all flip flops go to a 0 i.e. counter reset to zero, to be ready for next count.

It remained to explain when $Q_D$ goes a 1. We observe from the truth table that flip flop D never changes its state during counts 1 through 7. This is because at its clear input, $C_1$ a sustained 1 is always present on account of either $Q_B$ or $Q_C$ (or both) being 0 when $Q_A$ drops from 1 to 0. Thus input of D remains high and $Q_D = 0$. But after count 7, this high clear input is removed and $Q_D$ goes high (a 1) when $Q_A$ goes from 1 to 0. This happens at tenth pulse. The result is that FF/B is inhibited

DATE __/__/__

And counter reset itself. It may be remembered that such a reset condition is achieved only after the application of 16th pulse in a scale of 16 counter.